Glass Panel Processing for Electrical and Optical Packaging

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Abstract

Glass is a perfect substrate material for electrical and optical packaging. The integration concept to bridge board and chip level using thin glass substrates by lamination in between of PCB base material will be presented. Different thin glasses are commercial available and will be reviewed. Furthermore the paper reviews glass panel processing in the area of display and electro/optical packaging focusing on integration advantages for photonic packaging. Ion exchange technology for large panel processing to integrate high-performing optical waveguides will be demonstrated for multi-mode beam propagation. Based on glass based photonic system-in-package (SiP) which is done on wafer level the up scaling on panel size of those processes is discussed in detail and experimental results are presented.

Introduction

The increased demand for electronic substrates that meet the performance requirements of high density packages is leading research towards materials with improved properties compared to conventional organic laminates. These organic laminates (e.g. FR4) offer cost effective and large panel packaging but the integration potential is limited because of dielectric properties and dimensional instability under thermal load. Today 3D integration using silicon focuses on stacking of electronic chips to gain increased performance and bandwidth, reduced power consumption and form factor. Thus the state-of-the-art for wafer level processing (WLP) is a 300 mm silicon processing line. Silicon is widely used for electrical packaging because of mature CMOS technology and the established processes and tools but its semiconductor properties are a limitation because electrical circuits on surface and through-vias (TSV) need an insulation layer between. Furthermore photonic and MEMS heterogeneous integration have attracted much attention owing its high functionality, high-speed communication, and low power consumption [1].

An alternative for silicon or organic based interposer is a glass interposer having the same pitch size and accuracy as the highly integrated components that will be assembled. The coefficient of thermal expansion (CTE) of glass matches perfectly with silicon dies and makes the package more reliable. This approach was firstly proposed in 2008 [2,3] and is called "*glassPack*". The transparency of the glass have been enabled new integration architectures using direct "optical vias", for example electro/optical transceiver modules for on board assembly called "active interposer" [4]. The added value of glass substrates compared to other materials is the integration of high-performing optical waveguides that was presented for multi and even single-mode beam propagation on chip and board level [5]. Such interconnection technology became necessary since the demand for module and system performance increase asks for heterogeneous integration of photonic circuits with electronic circuits.

The paper is intended to propose the system concept and suitable technologies merging "*glassPack*" based active interposers with integrated optical waveguides with thin glass based EOCB [6]. So a recently developed glass based photonic SiP process is discussed shortly. After that the up scaling to large panel optical waveguide layers laminated in between PCB base material will be described. Additionally the paper reviews glass panel processing in the area of display and electro/optical packaging focusing on cost reduction and integration advantages.

Electro/optical system integration concept

Electro-optical circuit boards (EOCB) are a promising approach to overcome the intra- system bandwidth interconnection bottleneck in high performance systems.

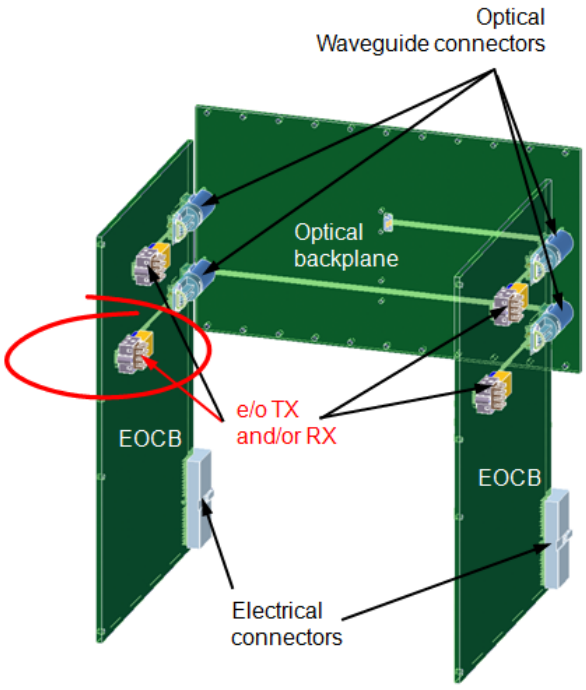

Figure 1: Schematic drawing of a demonstrator system with 2 modules per daughter card, and embedded glass double layer optical waveguides realized within the FutureBoard-Project [6] (drawing courtesy of R. Mödinger, ERNI electronics GmbH). The highlighted area depicts the focus of the paper at hand: Tx/Rx integration into large panel EOCB.

The architecture in **Figure 1** can be regarded as a basic one providing two (or more) pluggable Tx and/or Rx modules per EOCB daughter card. 90 degrees light deflection is required for the optical interfaces on daughter cards and backplane, respectively. The backplane can be separated into an optical (as displayed in Figure 1 only) and an electrical part for simplicity reasons but it can be integrated also. As indi-

cated in the middle of the optical backplane in **Figure 1** MT based optical outputs for fiber connectors are feasible at the backplane also.

The transparency of glass allows not only the planar integration of optical waveguides, but also lenses and beam steering units. **Figure 2** illustrates the envisioned glass based packaging approach for optical chip-to-chip interconnects. The illustrated package consists of a through-glass-via (TGV) interposer with electrical and optical interconnects that is mounted on a polymer based electrical-optical circuit board (EOCB) having thin glass layers with optical interconnects as well. We call this generic packaging concept "*glassPack"* as introduced recently in [7,8,9]. (Lens integration is described more detailed in another paper at the same conference).

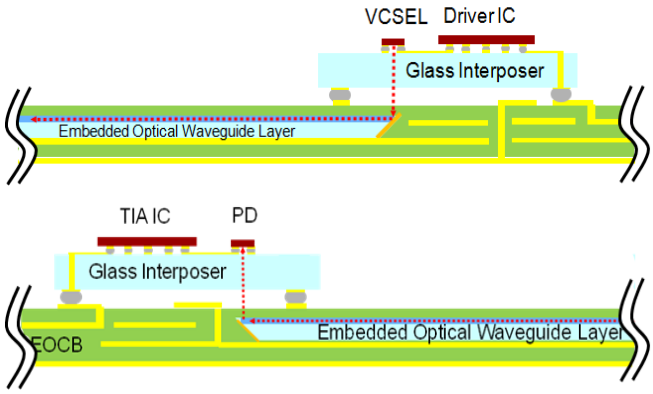

Figure 2: Schematic drawing of integration concept: parts of electro-optical PCB (EOCB) with embedded waveguide layer and *glassPack*: bare die assembled electro-optical Tx (top) and Rx (botton) located close to processor unit using glassy active optical interposer.

An already realized 40 Gbps transceiver module based on the *glassPack* approach was presented in [10] and is shown in **Figure 3** depicting the horizontal optical pathways for EOCB interconnection.

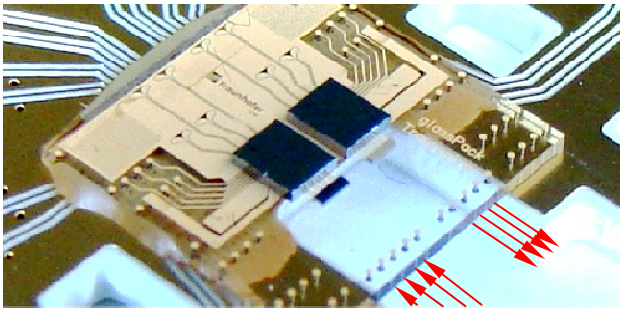

Figure 3: Optical photograph of parallel 4 x 10 Gbps optoelectronic transceiver module demonstrator mounted on a PCB. The arrows indicate the optical in and out pathways underneath of the glass interposer due to 90 degrees optical deflection. Waveguide pitch is 250 µm.

Characteristics of commercially available thin glass

An immense amount of different glass brands are offered by the glass industry today to meet custom specific requirements. Different glasses are necessary for different physical and chemical specifications which are required by different applications. For example glasses which have to be processed by ion exchange for waveguide integration needs a high alkaline content in the glass matrix. A glass which has to be bonded with silicon (wafer bonding or flip chip) requires a CTE of around 3 ppm K^{-1} to avoid stresses caused by CTE mismatch. Glass in wafer formats is fully compatible to wafer level packaging (WLP) lines. There is no difference between processing silicon wafer compared to a glass wafer except the lower thermal conductivity which requires optimization for hot-plate processes. The wafers are available with edge treatment with C- or facet shape. Schott AG offers thin glasses especially developed for target applications like AF32™ for electronic packaging or D263Teco™ for touch display manufacturing. Also Corning Inc. has thin glass sheets in the portfolio like Eagle XG slim™ or Jade™ for flat panel display or Gorilla™ for touchable display manufacturing. Thin glass sheets are manufactured by a down-draw process. The glass thickness is dependent on the manufacturing. For the down-draw process the minimal glass thickness (e.g. 30 µm for D263Teco™) is much smaller than for the micro-float or up-draw process but can be reduced by surface polishing to a final thickness of around 500 µm for instance. Down-draw material can be used without additional surface treatment, while the other glass types require a surface treatment (grinding, lapping, polishing) to meet surface quality requirements. Today, display manufacturing in a Gen 10 fab use thin glass in a scale 2850 mm x 3050 mm having a thickness of 700 µm [11].

Of course, display glasses are also used for other applications and available in wafer size and smaller thicknesses. 500 µm thick wafer of down-draw material with fire polished surface have typically 300 µm warp, < 10 µm total thickness variation (TTV) and average surface roughness (R_a) below 1 nm. Lapped and polished quality can go up to 80 µm warp, 2 µm TTV and < 1 nm surface roughness [12]. Beside down-drawn glasses other glass types like Lithosil™, B33™, B270™, Pyrex™ are widely used for MEMS, sensing and electronic packaging applications. The required surface quality is realized by lapping and polishing. As a result that kind of glass is only available on wafer or small panel size and not suitable for cost effective large panel processing.

A selection of commercially glass brands suitable for glass based packaging offered by Schott AG and Corning Inc. are summarized in **Table 1**. B33™, AF32eco™, Pyrex, Eagle XG slim, Jade has a CTE matches to silicon ICs which is beneficial to high reliability of solder joints. The integration of optical functions inside the substrate using the ion exchange technology requires an adequate alkaline content provided by glasses like D263Teco, B270™, Gorilla, B33, Pyrex, 0211™. Furthermore glass has excellent dielectric properties as well as ceramic materials that are often used for high-frequency applications (Al_2O_3: $\varepsilon_r = 9.6$, $\tan\delta = 5 \cdot 10^{-4}$).

Table 1: A selection of commercially glass brands suitable for glass based packaging offered by Schott AG and Corning Inc.

Company	Schott AG					Corning Inc.				
Brand	**Litho-sil**	**B33**	**B 270**	**D 263T eco**	**AF 32 eco**	**Pyrex**	**0211**	**Eagle XG slim**	**Gorilla**	**Jade**
Type	fused-silica	boro-silicate	crown-glass	boro-silicate	boro-silicate	boro-silicate	boro-silicate	boro-silicate	boro-silicate	boro-silicate
Process	micro-float		up-draw	down-draw		micro-float	down-draw	down-draw	down-draw	down-draw
Process Thickness	700 µm	700 µm	800 µm	30 µm	100 µm	700 µm	50 µm	<400 µm	500 µm	n.a.
Format	Panel and wafer					Panel and wafer				
Alkaline Content	alkali-free	4 wt%	17 wt%	13 wt%	alkali-free	4 wt%	13 wt%	alkali-free	n.a.	alkali-free
CTE	0.5 ppm	3.3 ppm	9.4 ppm	7.2 ppm	3.2 ppm	3.3 ppm	7.4 ppm	3.2 ppm	9.1 ppm	3.8 ppm
tanδ (1MHz)	14·10–4	37·10– 4	n.a.	61·10-4	28·10-4	50·10-4	46·10-4	30·10-4	100·10-4	20·10-4
ε_r (1 MHz)	3.8	4.6	7.0	6.7	5.1	4.1	6.7	5.3	7.3	6.0

But ceramic suffers from high surface roughness which increases high-frequency losses. In contrast, glass has excellent surface quality with R_a below 1 nm which makes it attractive for high-frequency applications. In summary, the right glass has to be selected dependent on the process and application. The presented glass brands are state of the art but further glass compositions will be developed depending on the market needs.

Review on flat panel display manufacturing

The crowing display industry processes glass panels having a size of 2.2 m x 2.5 m by using thin film deposition, lithographic processing, stacking and cutting. For those large panels having a thickness between 0.5 mm and 0.7 mm all processes are automatic in a fabrication of generation 8.

Due to the fast increasing market of flat panel display (FPD) applications like LCD during the last decade in Asia there are production lines available to process continuously enlarging glass panel sizes with increasing resolution. The main processes are described in the following.

In order to structure the large panel substrates *resist coating* and metallization by *sputtering* is essential and can be realized. *Spray coating* and *dip coating* are common technologies and sputter machines can handle large substrate sizes with sufficient homogeneity.

Maskless lithography is necessary to avoid high mask costs and can be implemented using electron beam, laser direct writing, or laser direct imaging (LDI) technology. Laser direct imaging technology is suitable for pattering of very large sized FPD panels like more than 100 inches PDP and LCD. In addition, adapting of LDI technology has a lot of benefits like fast exposure speed using multi-array optical engines, and using 405 nm wavelength semi-conductor laser which has eight times longer life time than the conventional UV lamps [13].

Cutting wheels and lasers are used as the two main tools for *glass cutting*. The former is a mechanical way of cutting the glass substrate. It uses one (or two) cutting wheel to scribe the glass surface and then the substrate is cleaved using a mechanical stress method. The latter utilizes an ultraviolet (UV) laser with a wavelength of 266 to 355 nm for the scribing of the glass substrate, and then by the same process as the former [14]. For smaller substrates sawing processes can be adopted from wafer level packaging. Here a twin process from both sides simultaneously is advantageous to reduce any cracks at the edge resulting in chippings and breakages.

Despite of the Asian dominance in very large FPD manufacturing today there are diverse companies worldwide developing and producing FPD for special applications like automotive, industry, and telecommunication. Here we see many chances to converge mature technologies with new application scenarios as proposed above.

Electrical packaging using thin glass panels

In this paper the *glassPack* concept will be presented combining the optical properties of glass with integration capabilities on module and large area board level (EOCB). In this chapter some of the most important arguments for using glass from an electrical and reliability point of view will be mentioned.

Due to the fact of the increasing requirements in thermal and mechanical stability in PCB´s it is promising to laminate thin glass foils in between the conventionally used substrate layers or in a symmetric lamination built up (**Figure 4**). Without any further processes the thin glass sheet reduces the CTE of the base material and the PCB, respectively. In order to achieve an optical functionality the laminate has to be equipped with optical deflection elements and cavities.

Due to its optical transparency glass enables clear observation of buried circuit layers, so that improved alignment accuracy can be achieved when structuring vias, thereby reducing the size of capture pads and enabling the reduction in pitch of the devices to be assembled [3].

Based on these arguments it seems to be straightforward to propose the possibility of EOCB made from thin glass layers only or with minor polymeric base material for mechanical reasons. From this point of view the integration potential of glass bridging the gap between chip and board becomes obvious. Glass based SiP and board level packaging can be merged technologically with inherent optical integration capability in the multimode and single mode domain.

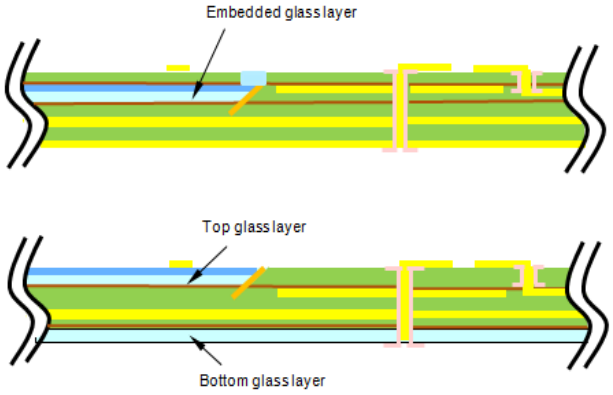

Figure 4: Schematic drawing of *glassPack* based integration concept showing EOCB only with to basic build ups of embedded waveguide layer (glass core built up, top) and surface laminated glass sheets (glass surface built-up, bottom).

Crucial is the selection and suitable combination of appropriate glass laminates, reinforcing materials and resin, as well as the rheology of the resin and the pressing cycle for lamination. No reinforced systems such as coated copper foil (RCCF) are known as well-suited, in conjunction with a suitable resin rheology, for being pressed with glass to create a laminated composite. In reinforced types, a prepreg is pressed with copper foils on one side and a glass film on the other. It has been shown that the type of reinforcing material and the resin system used have a major influence on the results of pressing. For instance, standard glass fabric is not suitable, because it results in a strong tendency for cracks to form in the glass film probably due to knots in the fabric [15].

Optical packaging using thin glass panels

The need of optical waveguides in next-generation high-end data processing systems such as Internet switches or servers are predicted for one decade. The dimensions of optical backplanes in such systems are up to 1.4 m x 0.7 m and the optical loss of waveguides should be less than 0.1 dB/cm. Furthermore all the used materials and integrated optical structures have to withstand the process conditions of the following board interconnection and surface mount technologies. [16]

Worldwide a scientific state in waveguide technology on wafer level is usual and well described in detail, but for commercial use on board and backplane level process equipment is only partially available (e.g. flat panel display technology) and has to be adopted completely for a successful technology transfer. Important steps in research and development have been done at Fraunhofer IZM. Started from a standard process on wafer level the board level capability is achieved and results are presented in the paper on hand. The approach to backplane level is going on. The major role on this way plays the up scaling of the very precise wafer level technology to an economic backplane technology that fits today's commercial board interconnection and surface mount technologies.

The optical waveguides in thin glass can be fabricated by thermal silver ion exchange processes in molten salt bath. Following some of the most important issues are summarized:

The main technology requirements for up-scaling substrate size of optical waveguide layers are:

- Manufacturing of diffusion masks and alignment marks using thin film aluminum deposition on the thin glass surface,
- Different ion-exchange process steps to form planar integrated waveguides,
- Separation techniques for cutting the optical layout,
- Characterization of optical waveguide performance.

The technological challenges for up scaling are:

- Economic and green manufacturing,
- Integration in printed circuit board technologies,
- Available equipment

In particular:

- Resin coating of photosensitive resist
- Structuring of smooth waveguide bending
- Up scaling of the molten salt bath
- Process homogeneity ion-exchange over panel size
- Refractive index distribution
- Intrinsic losses
- Stress compensation
- Separation on board level

Experimental results

In close collaboration with the German PCB manufacturer Contag GmbH, Berlin, the PCB integration of thin glass to form large panel EOCB was investigated. The results concerning the main manufacturing steps and specific challenges are presented and discussed in the following;

Lamination: In contrast to former approaches we have been concentrated on build-ups with thin glass lamination covering the full 210 mm × 297 mm size of the panel. This is much more challenging then the partly embedding of smaller waveguide sheets as used in [6]. Lamination direct in between RCCF works without any problems as assumed. As can be seen from ultrasonic investigations in **Figure 5** no cracks arise. The sticking is very good.

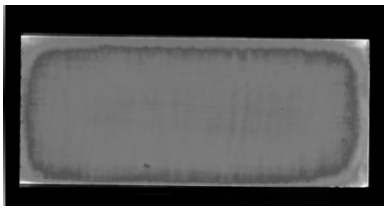

Figure 5: Ultrasonic image of 200 mm x 80 mm thin glass foil laminated in between RCC foils.

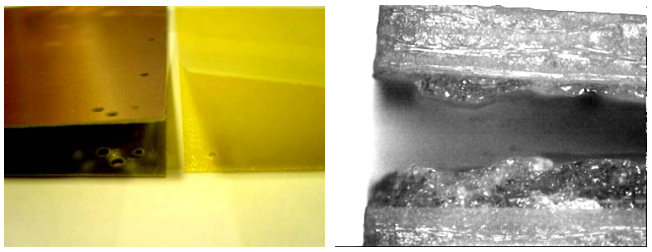

Figure 6: Photograph of two delaminated glass core build-ups using FR4 (left). The delamination is caused by lateral glass damaging (right) (figures courtesy of Contag GmbH).

In case of base materials like FR4 it was found that after cutting, micro cracks at the edge cause delamination under certain circumstances mainly in the glass core built-up after time due to frozen stresses resulting from different CTE of the materials. From **Figure 6** (right) it became obvious that really no sticking problems arise but lateral damaging of the thin glass sheet itself. The process optimization dealing with different base materials and lamination conditions was successful as can be seen in **Figure 7.**

Figure 7: Optical photograph of laminated thin glass sheet in glass core build-up using FR4. Size is 210 mm × 297 mm with small frame. The 3 open releases are milled and show no delamination after time (figures courtesy of Contag GmbH).

Drilling is a crucial process risk and has been investigated carefully. There is a huge amount of parameters which can be played with. The goal is a high quality and small diameter hole able to be metalized without any failures. The problems coming up are related to the different hardness of the glass and the base materials, respectively, causing chippings and breakages at the glass edge.

In **Figure 8** results from glass surface built ups (see schematic drawing in Figure 4) are shown. These results show already a good quality. The results achieved for glass core built ups are even much better due to polymer supported glass edges during the machining. For optical coupling the glass core built-up needs additional plasma etching to open the polymeric top layers of the EOCB which was find to be possible using standard etching parameters.

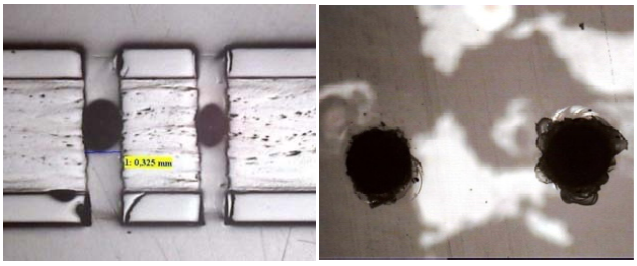

Figure 8: Optical photograph of two drilled holes in glass surface build-up. The diameter is 300 µm. The pitch is about 1 mm. Small cracks at the bottom edge arise (figures courtesy of Contag GmbH).

Milling is necessary to open releases as can be seen from **Figure 7** and in order to prepare the optical interface in the waveguide region, respectively. This machining tends to cause additional cracks causing the already discussed lateral damage of the thin glass layer. Thus the glass core built-up is critical according to the above discussed argumentation. On the other hand the bare glass edge is jeopardized to be damaged as can be seen in **Figure 9** (left). Process optimization on both built ups are possible to achieve sufficient qualities.

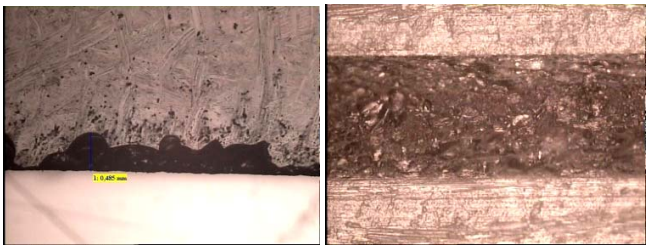

Figure 9: Optical photograph of milled (but not polished) glass edges with damaging (glass surface built-up, left) and without (glass core built-up, right) (figures courtesy of Contag GmbH)

Laser structuring is besides mechanical machining very common in PCB manufacturing and has been evaluated in terms of suitability for the large panel EOCB. Same as found in the mechanical machining experiments the glass core built-up remains more advantageous. Holes for through vias where successfully structured as shown in **Figure 10.**

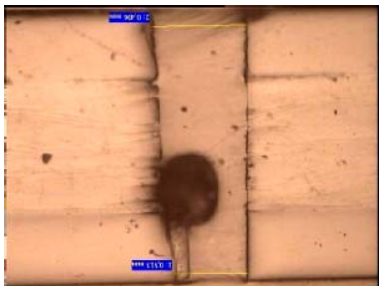

Figure 10: Optical photograph of a via hole of about 300 µm diameter (glass surface built-up).

As inherent to laser technology the holes have a conical shape. But aspect ratio achieved is suitable for galvanic metal-

lization. The top and bottom edges of the holes show satisfactory quality (**Figure 11**).

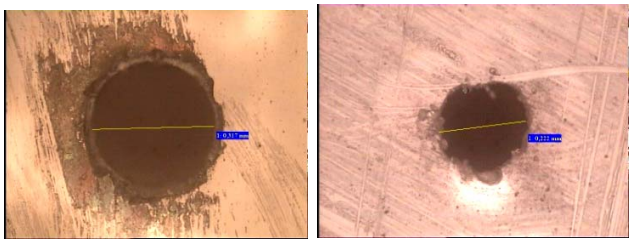

Figure 11: Optical photograph of a laser drilled via hole of about 300 µm in diameter at laser inlet (left) and about 220 µm at laser outlet (right) side (figures courtesy of Contag GmbH).

The following section describes the results related to the scaling of the optical waveguide technology to large panel sizes. The differences and challenges are compared in Table 2.

Table 2: Waveguide process scaling from wafer level to large panel technology

Process	Target	Wafer Level	Board Level
Resin coating	High resolution development, avoiding of resin dissipation, low dose for fast UV-exposure	Spin coating	Solid resist lamination, dip coating
UV-exposure	At least 20 microns diffusion mask opening for smooth MM-waveguides ,	Mask exposure	Laser direct pixel imaging, Laser direct vector imaging
Thermal ion exchange	Optical waveguide structuring, safe handling, mechanical improvement for further treatment (characterization, lamination), homogeneity	standard oven	Remote control for batch processing, handling automatization
optical end face preparation, seperation	Cleave without micro cracks, optically grade and mechanically reliable	Dicing, cleaving, polishing, laser structuring	CNC milling and cleaving, laser cutting
Functional test	Quality control, optical transmission and loss characterization	Automatic loss measurement	Automatic loss measurement

For wafer level processing spin coating is applied as depicted in **Figure 12.** For the dip coating an in-house newly developed coater has been realized able to handle large thin glass sheets using motor-driven and controllable feeding (**Figure 14**) The process results in about 6 µm thick resist films as can be derived from **Figure 13**.

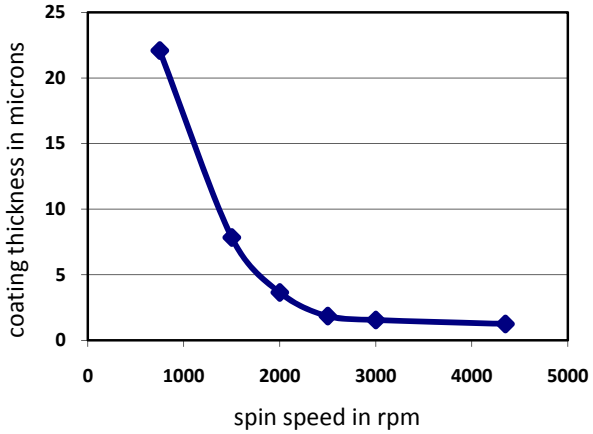

Figure 12: Spin coating thickness in dependence of the spin speed. For higher speeds than 3000 rpm the thickness remains finally at 1.25 µm using AZ 4562 Clariant resist.

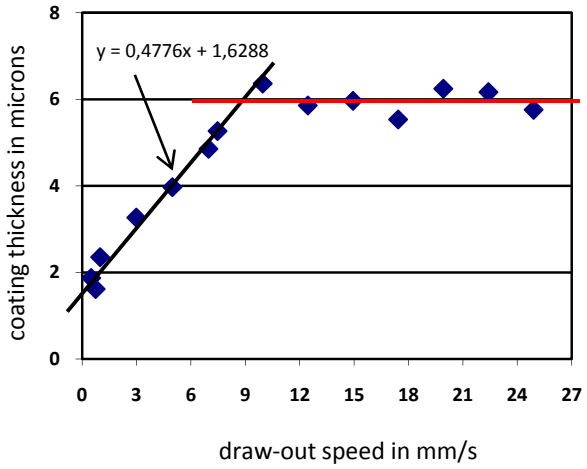

Figure 13: Dip coating thickness in dependence of the draw-out speed. For higher speeds than 9 mm/s the thickness remains finally at 6 µm ("MC Dip Coating Resist", MicroChemicals, minimal thickness 1.8 microns).

Figure 14: Optical photograph of newly developed dip coater for thin glass sheets.

The test pattern to compare wafer and large panel lithography processes is depicted in **Figure 15**. Beside straight ones also bended waveguide structures have been realized according to shapes at formerly used wafer masks for better comparison.

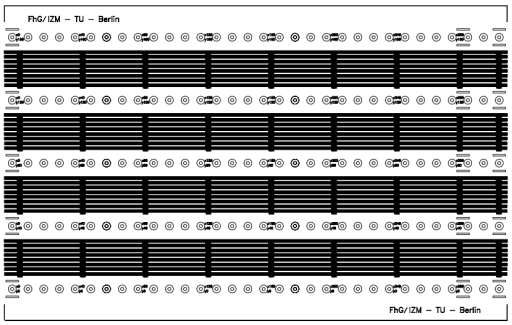

Figure 15: Straight waveguide layout for large panel processing.

The problem for large panel patterning of optical waveguide structures is achieving as high resolution as feasible at wafer level. In **Figure 16** (left) the high quality edge of a diffusion mask opening is shown. The bending of the splitter structure does not show any steps or stitches. But high precision masks are not an option due to cost reasons. So digital imaging using UV-laser light comes out as the most suitable technology. It works very well for straight waveguides but problems arise if bendings shall be realized. In **Figure 16** both approaches can be compared. On the right hand side the stitches due to digital errors of the pixel UV-exposure at bendings can be seen clearly. After wet chemical aluminum etching the glass sheets are ready for thermal ion exchange (**Figure 17**) in a hot salt melt reactor.

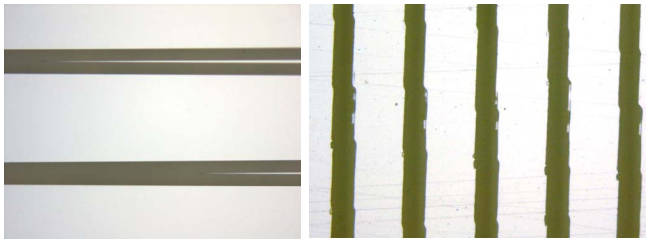

Figure 16: Optical photograph of diffusion mask detail with waveguide bended splitters, patterned by mask exposure (left) and LDI pixel exposure with "Orbotech Paragon 9000" (waveguide pitch is 250 µm).

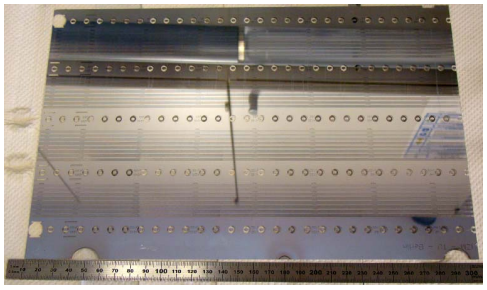

Figure 17: Patterned aluminum diffusion mask on 210 mm × 297 mm glass panel ready for 1st ion exchange process.

It was necessary to newly develop an ion exchange reactor in-house able to handle such large thin glass sheets using motor-driven and controllable feeding. In **Figure 18** the diffusion bathes in the lower and the feeding mechanism at upper part are depicted.

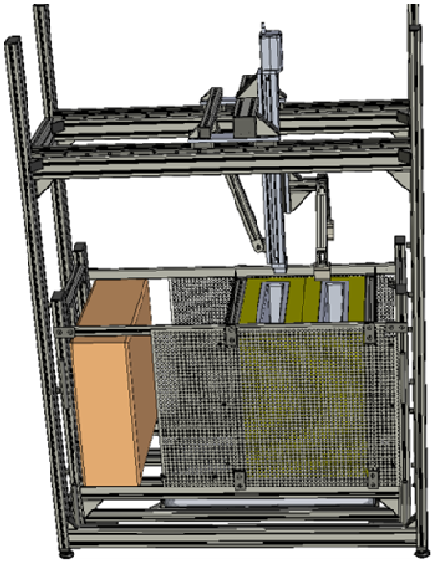

Figure 18: Design sketch of the large panel ion exchange reactor for thermal ion exchange used to produce the optical waveguides.

As detailed described in [6] the first ion exchange step is followed by diffusion mask removal and a second thermal ion exchange causing buried waveguides by silver depletion at the surface. After that the glass sheets can be cleaved if desired for further processing as shown in **Figure 19.**

Figure 19: Mechanical cleaving using standard equipment.

Optical test of high canal count waveguide sheets requires automated loss measurement capabilities. The used high precision station is shown in **Figure 20** using fiber optical probes.

The loss measurement results achieved at 850 nm for large panel waveguides having a length of about 150 mm are between 0.2 and 0.3 dB/cm. Main loss reasons are etch mask failures and area inhomogeneities within the ion exchange process itself. As can be seen from at 1310 nm and 1550 nm the attenuation can be expected to be smaller.

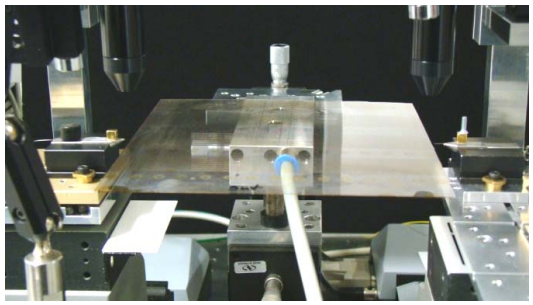

Figure 20: Test station for automated optical waveguide loss measurement to ensure final prototype quality.

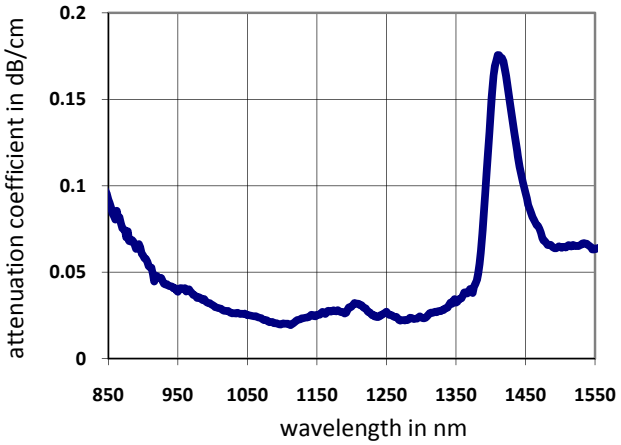

Figure 21: Spectral attenuation for multimode waveguides measured at wafer size samples.

Conclusion

We carried out technology testing to show the feasibility of thin glass foils for large panel. The crucial point was to scale the wafer level technologies which have been already proven to large panel EOCB technology. We have been focused on optical integration and PCB manufacturing. For the first time optical thin glass layers of 210 mm × 297 mm size have been functionalized optically by thermal ion exchange. The optical attenuation is still higher than on wafer level but optimization is in promising progress. The most important impact can be gained by improving diffusion mask patterning. Here laser direct imaging seems to be the most promising approach in ongoing investigations. There are many processes which can be adopted from FPD manufacturing.

The PCB manufacturing results show the feasibility for large panel integration. Lamination, drilling, cutting and milling have been investigated and validated. The glass core built-up seems to be the most reliable one.

Future work will be on assembly and integration of SiP modules as shown in Figure 3 on glass integrated EOCB. Particularity reliable soldering and optical interconnection have to be further developed in order to complete the integration of *glassPack* made modules into EOCB.

Since the interest on SiP solutions will increase in the next years the integration of optical, fluidic, and electronic applications into one system will be an ongoing development on wafer level. Our packaging solution is perfectly suitable for 3D heterogeneous integration and realization of complex and reliable microsystems assembled on EOCB. The benefit of glass for both module and board level results in excellent optical, electric, chemical, and thermal properties. In particular the optical pathways can be realized using one material and technology platform. Other functions like mechanical and low frequency can be satisfied by conventional packaging.

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